Vertex Detector Off-Detector Electronics (ODE)

TTC Link (optical)

Analog Data Links (twisted pairs)

Front-End Readout

TTCrx

Clk Phase Control

FADC

8 bit

Reset
Clock
L0Accept
L1Accept

Front End emulator

Synchronization and event tagging logic

Pedestal subtraction

Baseline Correction

Hit finding

Cluster encoding

L1 Buffer

Parameters
FPGA config

JTAG I^{2}C Other

DCS interface

L1 decision logic and
L1 Buffer read-out

Formatting

L1 Link Interface

VT Link Interface

Control/Monitoring

Trigger Preprocessor

Cavern

Counting room

L1 Link Interface

L1 Data Processing
(zero suppression)

DAQ interface

DAQ Preprocessor

DCS Link (Local IOS)

(CANbus/VMEbus)

FE Link (to RU)
(S-Link)

VT Link (to L1 trigger)
(S-Link)

Yuri.Ermoline@cern.ch

ODE Design

VHDL/FPGA design flow:

- **VHDL entry**   **text editor/VisualHDL**   **Summit**
- **VHDL simulation**   **Leapfrog VHDL simulator**   **Cadence**
- **FPGA synthesis**   **Altera MAX+PLUSII**   **Altera**
- **FPGA place&route**   **Altera MAX+PLUSII**   **Altera**
- **FPGA configuration**   **Altera Programmer**   **Altera**

ODE Design Lab:

- **Sun (VHDL entry, simulation, FPGA synthesis, place&route)**
- **PC (FPGA configuration, VME interface)**
- **Altera stand-alone programmer**
- **National Instruments VME-PCI8015 MXI-2 Kit for Windows NT**
- **TTC mini-crate + TTCrx evaluation board +TTCvi (H.Muller)**
- **HP16500A Logic Analyser & Oscilloscope**

Possible VHDL/FPGA design flow in the future:

- **VHDL entry**   **Renoir**   **Mentor**
- **VHDL simulation**   **ModelSim**   **Mentor**
- **FPGA synthesis**   **LeonardoSpectrum**   **Mentor**
- **FPGA place&route**   **Altera Quartus**   **Altera**
- **FPGA configuration**   **EEPROM+ISP/JTAG**   **Altera+?**
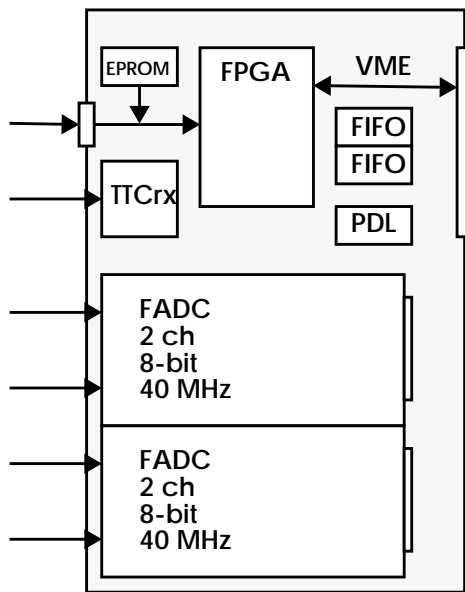
ODE Design Lab Extension:

- **SCTA control environment (CORBO, Sequencer, etc.)**
- **DCS evaluation kit (PCI interface, controller, SW)**
- **VT and L1 link evaluation setup**
- **DAQ Preprocessor demonstrator**
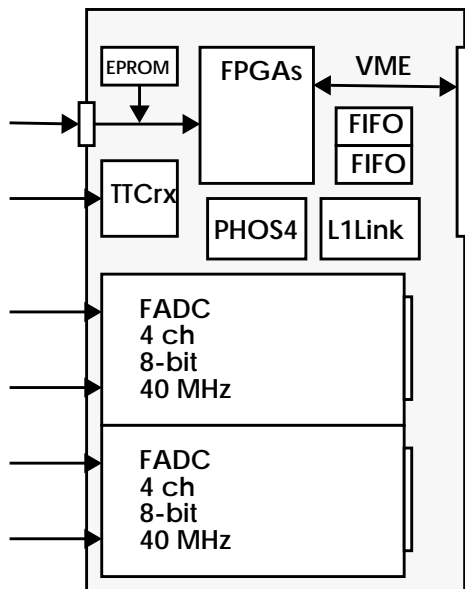
First ODE Prototype
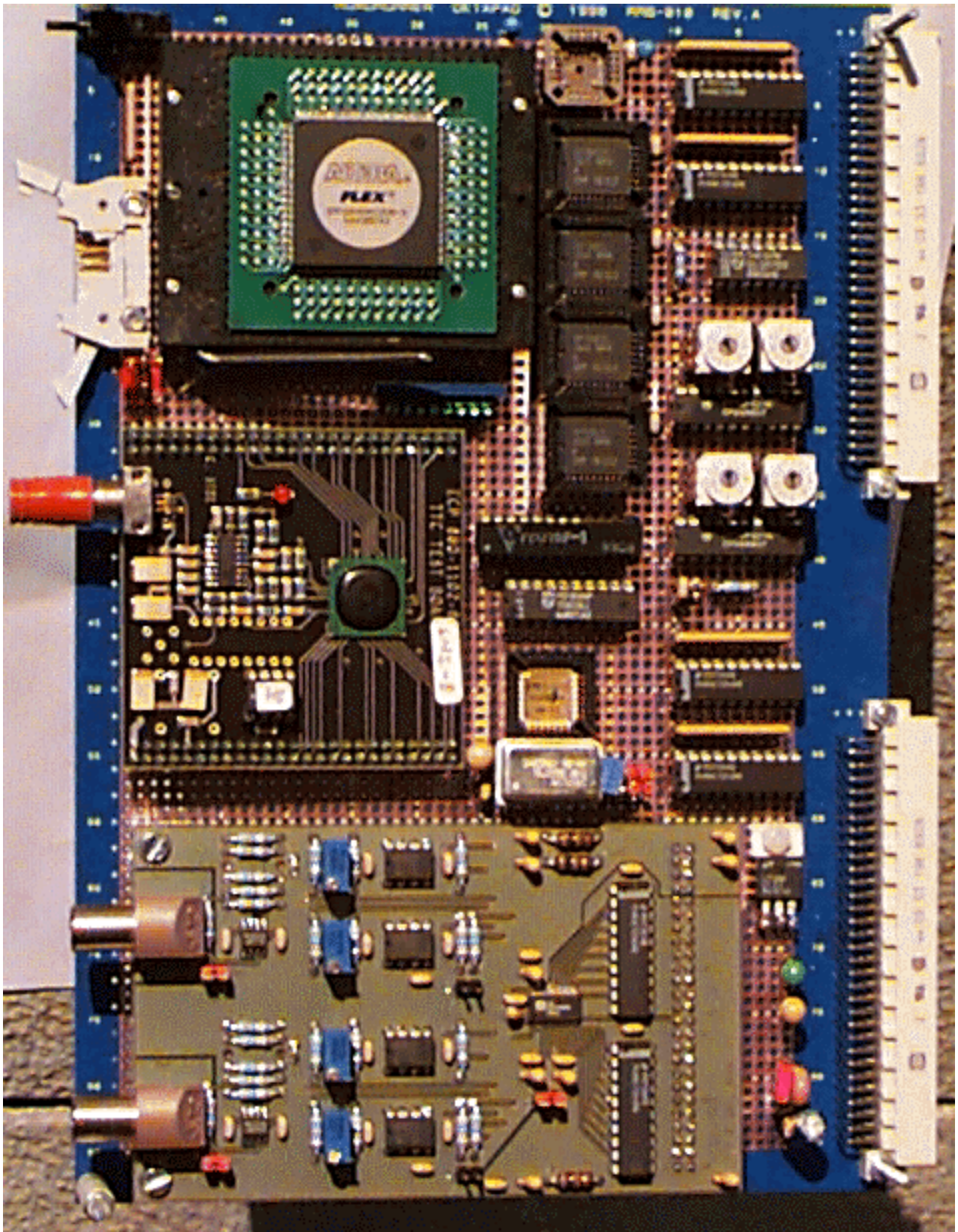
Front-End Read-out

1999

- Form factor: 6U VME
- Fast control: TTCrx (Clk, L0A)
- FADC: 4 ch 8-bit 40 MHz
- Phase control: PDL (9+31*1 ns)
- FPGA: 1 FLEX 10K50-240
  - VME interface, control
  - FADC data capture
  - Synchronisation
  - FE emulator
- L1 buffer: SyncFIFO 2K*32
- Slow control: VME A24:D32
- FPGA config: EPROM (EPC1)
                  download cable

2000

- Form factor: 6U VME
- Fast control: TTCrx (Clk, L0A)
+ FADC: 8 ch 8-bit 40 MHz
+ Phase control: PHOS4
+ FPGAs: 4 FLEX 10K50-240
  - VME interface, control
  - FADC data capture
  - Synchronisation
  - FE emulator
  - L1 decision logic
  1 FLEX 10K20-240
  - L1 Link interface
+ L1 buffer: SyncFIFO 8K*64
- Slow control: VME A24:D32
- FPGA config: EPROM (EPC2)
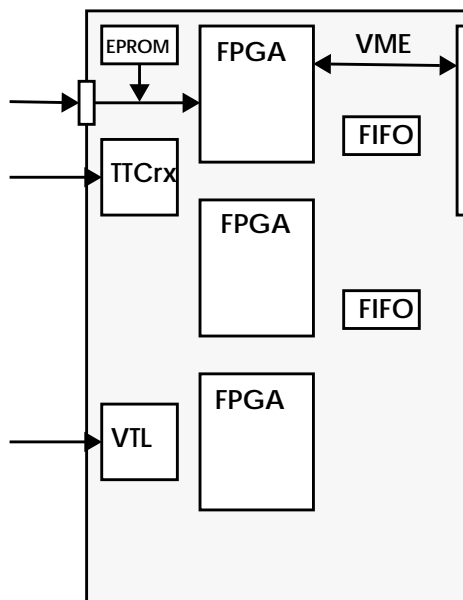   download cable

Control/Monitoring

2000
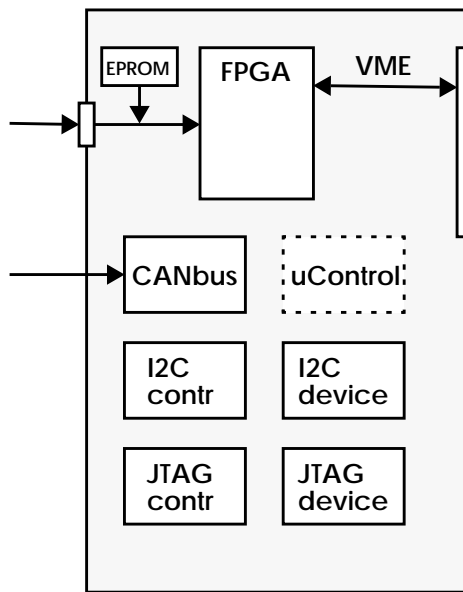
- **Form factor:** 6U VME
- **FPGA:** 1 FLEX 10K50-240
- **Slow control:** VME A24:D32

- General board control
CANbus/FPGA
- Parameters
CANbus/I2C
- TTCrx and PHOS4
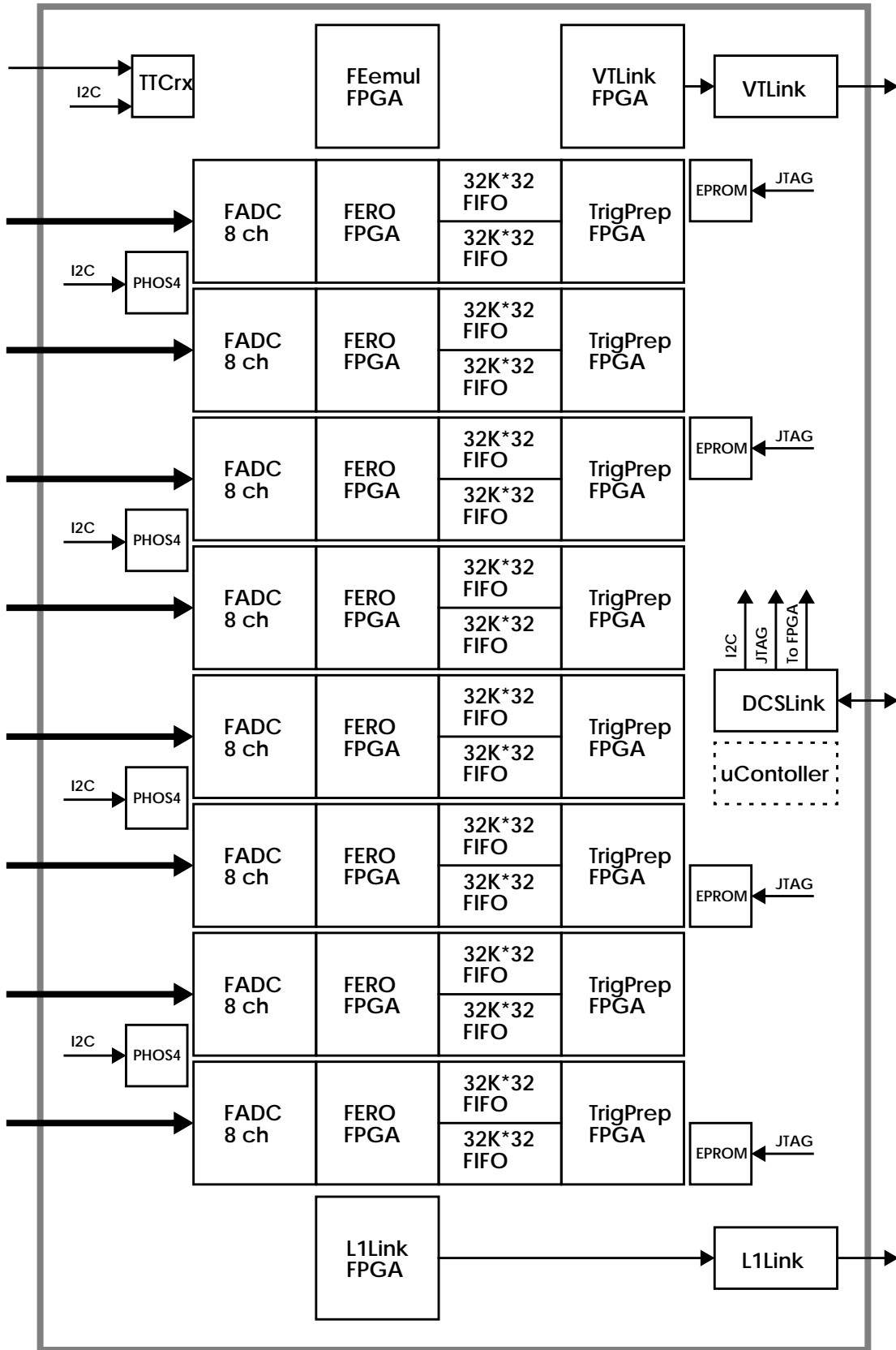**CANbus/JTAG**
- EPROM ISP

Trigger preprocessor

2000

- **Form factor:** 6U VME
- **Fast control:** TTCrx (Clk, L0A)
- **FPGAs:** 2 FLEX 10K50-240

- Trigger preprocessor (4 ch)
- VT Link interface
1 FLEX 10K20-240
- VT Link interface (VTL)

- **Input data:** FIFO 2K*32
- **Slow control:** VME A24:D32

64 channels ODE board layout

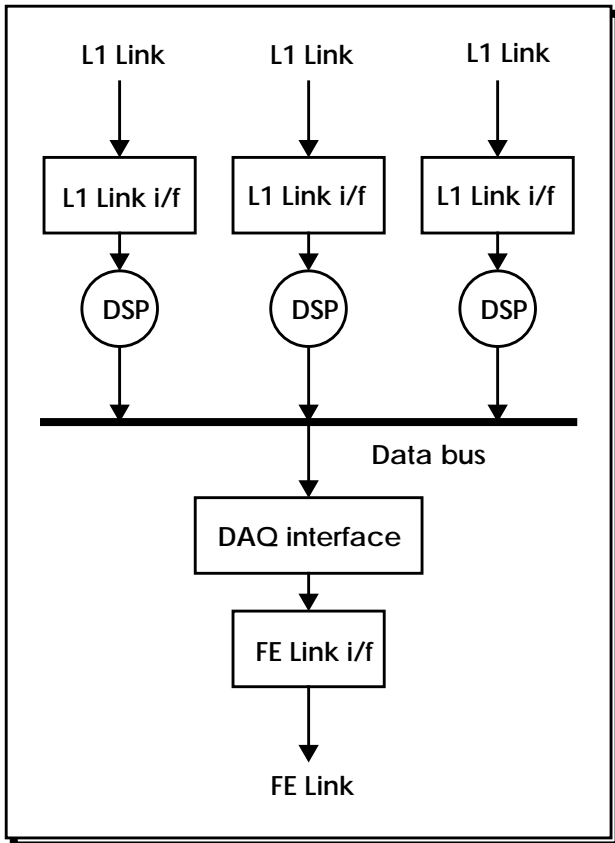**In the TP - one DSP per ~8 analog input links (258 VD channels)**
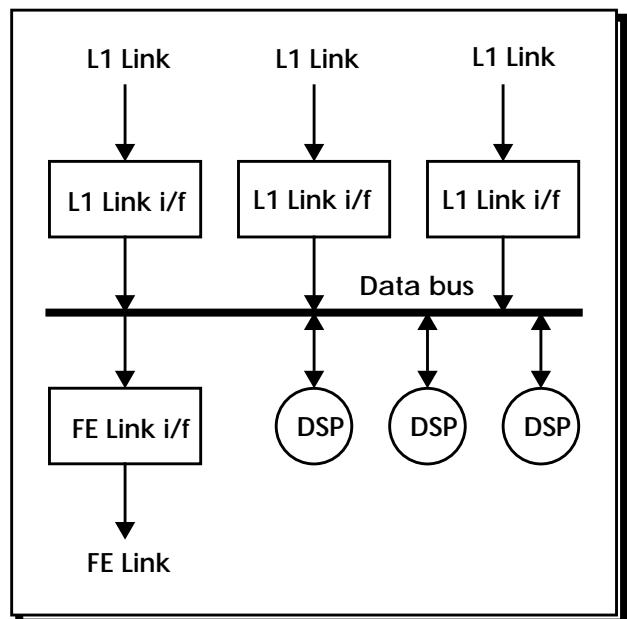**In total ~870 DSPs, ~11 MB/s input rate (8*32*40kHz) per DSP**

In a case of one L1 Link per ODE board (64 input links) ~85 MB/s
(without zero suppression) - in total ~110 L1 Links

What could be an architecture for the ODE DAQ Preprocessor?

L1 Link	L1 Link	L1 Link

L1 Link i/f	L1 Link i/f	L1 Link i/f

DSP   DSP   DSP

Data bus

DAQ interface

FE Link i/f

FE Link

E.g.: Compact PCI
     DSP cards
     I/O cards

E.g.: Multi-CPU board

L1 Link	L1 Link	L1 Link

L1 Link i/f	L1 Link i/f	L1 Link i/f

Data bus

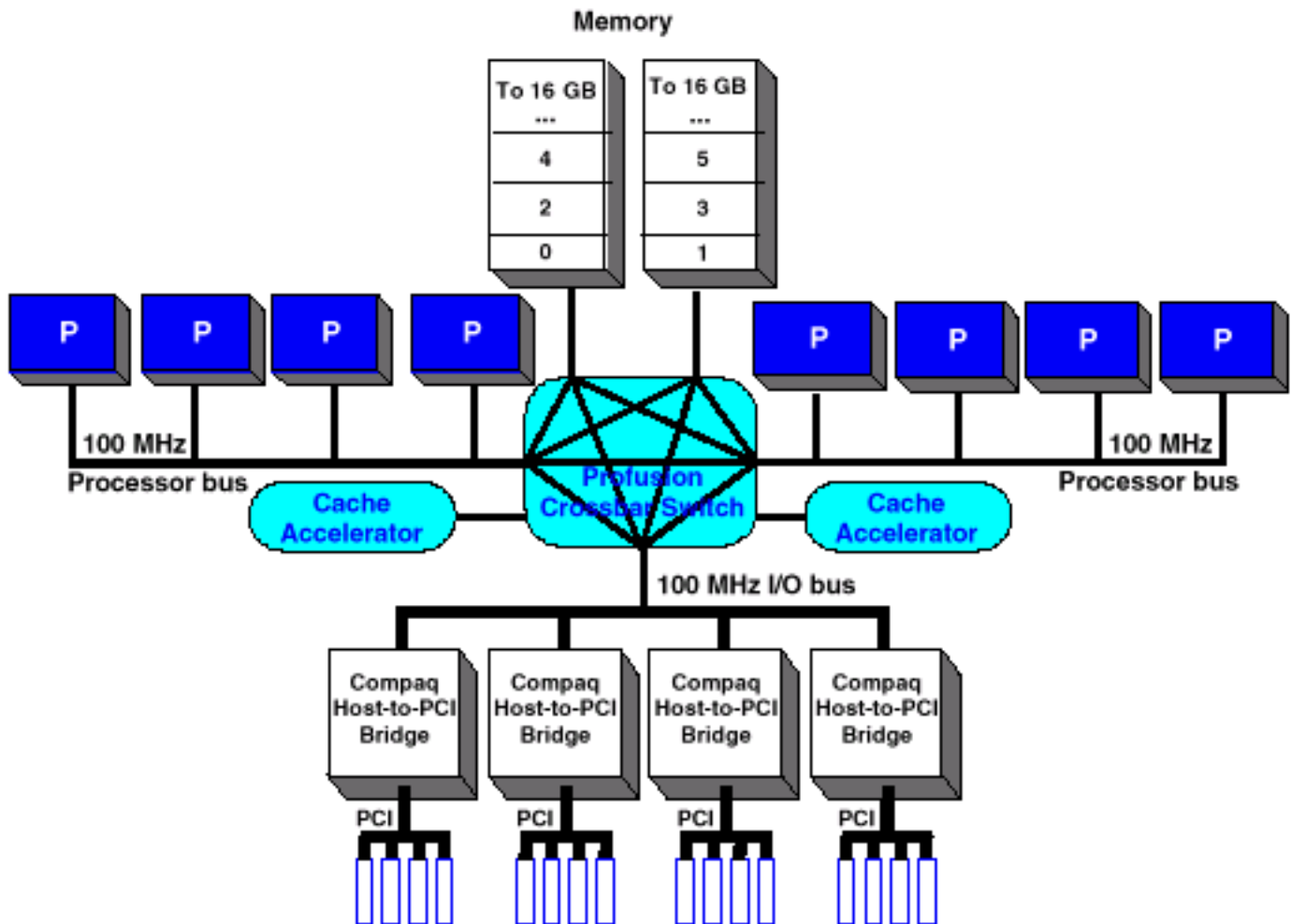FE Link i/f   DSP   DSP   DSP

FE Link

Figure 1: Block diagram of the Compaq 8-way SMP system architecture.

- Dual 100-megahertz (MHz) processor buses
- Dedicated 100-MHz I/O bus
- 8-way multiprocessing with Pentium III Xeon processors
- Multiported system architecture (five-point crossbar switch)
- Dual-ported, interleaved memory
- Uniform memory access for all eight processors
- Dual cache accelerators
- Up to four Compaq designed host-to-PCI bridges
- Up to 32 gigabytes (GB) of synchronous dynamic random access memory (SDRAM)